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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/956,994	09/21/2001	Mutsumi Kimura	110423	2948
25944	7590	06/02/2006		
OLIFF & BERRIDGE, PLC P.O. BOX 19928 ALEXANDRIA, VA 22320			EXAMINER LEWIS, DAVID LEE	
			ART UNIT 2629	PAPER NUMBER

DATE MAILED: 06/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/956,994

Applicant(s)

KIMURA, MUTSUMI

Examiner

David L. Lewis

Art Unit

2629

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 15 March 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-16 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>2/7/2006</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

- 1. Claims 1-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. (5349366) in view of Yamazaki (6545656).**

As in claim 1, 9, 10, 11, 12, 15, and 16, Yamazaki (366) et al. teaches of a driving method for an electro-optical device which includes, corresponding to an intersection of a scanning line, **figure 1A item Vg,**

and a data line, **figure 1A item Vd,**

a power line, **figure 1A item VLC,**

an electro optical element, **figure 1A item LC,**

a driving transistor that controls a current flowing through the electro-optical element, **figure 1A item Tr2**,

and a switching transistor that controls the driving transistor, **figure 1A item Tr1**,

the driving method comprising: a setting step of supplying a first on-signal to switching transistor via the scanning line, **figure 1B item Vg (t0)**,

and of supplying a set signal to select a conducting state or non-conducting state of the driving transistor to the driving transistor via the data line and the switching transistor in accordance with a period for which the first on-signal is supplied, **figure 1B item Vd (t0)**;

the driving transistor controlling the supply of power between the power line whose potential is constant and the electro optical element, **figure 1B item Vd (t1 to t2)**;

and a resetting step of supplying a second on-signal to the switching transistor via the scanning line, **figure 1B item Vg (t2)**,

and of supplying a reset signal to select the non-conducting state of the driving transistor to the driving transistor via the data line and the switching transistor in

accordance with a period for which the second on-signal is supplied, **figure 1B**
item Vd (t2),

wherein the period for which the first on-signal is supplied coincides with a period
for which the set signal is supplied, **figure items Vg and Vd, t=to.**

As in claims 1, 10, and 11, Yamazaki et al. (366) fails to explicitly teach of a
period of supplying the reset signal via the data line within a vertical scanning
period being substantially constant. **Yamazaki (656) teaches of a liquid crystal**
display having a plurality of pixel TFT's which are matrix disposed wherein reset
is performed during a subframe of the frame period, column 4 lines 8-60.

Further, Yamazaki (656) teaches of a period of supplying the reset signal via the
data line within a vertical scanning period (frame) being substantially constant,
figure 3 items 2nd Tsf and 4th Tsf. Said subframe feature of Yamazaki (656) is
applicable to the display method of Yamazaki (366) given both teach methods of
solving the problem of resetting a display. The drive method of Yamazaki as
shown in figure 1A and 1B can be applied to the subframe equivalent as taught
by Yamazaki (656).

Said known modification would provide for a period of supplying the reset signal
via the data line with a vertical scanning period being substantially constant in

view of Yamazaki's (366) figures 5-6, wherein a plurality of resets are performed within one frame period, as found in claims 1, 10, and 11.

Therefore it would have been obvious to the skilled artisan at the time of the invention to provide the reset signal as taught by Yamazaki (656) in the device of Yamazaki (366) because resetting a display is known to be useful to clear a display screen as taught by Yamazaki (656), and Yamazaki (656) further suggests said resetting can be performed within one frame period in a like device as taught by Yamazaki (366), as found in claims **1, 9, 10-12, 15, and 16**

As amended, as in claim 12 Yamazaki (366) fails to explicitly teach of the number of the signal to perform the setting step and the signal to perform the resetting step being substantially the same. Said feature would have been obvious to the skilled artisan in view of Yamazaki (656) as argued above given figure 3, wherein Yamazaki (656) teaches of the number of the signal to perform the setting step and the signal to perform the resetting step being substantially the same within a frame period.

As amended, as in claims 15 and 16, Yamazaki (656) teaches of a plurality of the pairs of the setting step and the resetting step being performed within one frame period, figure 3 items 1st to 4th Tsf, wherein the number of subframes would be an obvious design choice to the skilled artisan, at least two set reset

operations of the plurality of the set reset operation having mutually different time lengths,

As in claims 2 and 3, Yamazaki et al. teaches of, further including a horizontal scanning period that includes a first sub horizontal scanning period to perform the setting step, **figure 1B item Vd (t0-t0.5)**, and a second sub horizontal scanning period to perform the resetting step, **figure 1B item Vd (t0.5-t1)**.

As in claim 7, Yamazaki et al. teaches of, further including providing the set signal to be a signal for setting the conducting state for the driving transistor rather than the signal for selecting the conducting state or the non-conducting state of the driving transistor, **figure 1B item Vg (t1-t2)**.

As in claim 8, 13, and 14, Yamazaki et al. teaches of, further including driving the electro-optical element including an organic electroluminescence element, figure 1A item LC.

As in claim 4, 5, and 6, Yamazaki et al. teaches of wherein, further including obtaining a gray-scale by performing a plurality of set-reset operations, each set-reset operation including the setting step and the resetting step, column 16 lines 35-67, figure 6A, wherein said gradation is performed according to said method of claim 1.

Response to Arguments

2. Applicant's arguments filed 3/15/2006 with respect to claims 1-16 have been considered but are not persuasive. See the rejection over Yamazaki et al. in view of Yamazaki. Applicant argues Yamazaki 366 fails to teach of a transistor for controlling a current flowing through the electro optical element. The Examiner disagrees. Yamazaki 366 teaches of a thin film transistor Tr2, well known in the art to control current flow from the device drain to source when the appropriate threshold value is provided at its gate. Here in Yamazaki, when the appropriate pulse voltage is provided at the gate of Tr2, current is allowed to flow from drain to source of device Tr2, and as a result, the electro optical element is turned on. The device physics of the TFT (thin film transistor) is well known in the art and current flow is certainly a known element of said device as provided in TFT pixel displays. Rejection maintained.

Conclusion


3. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set

to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **David L. Lewis** whose telephone number is **(571) 272-7673**. The examiner can normally be reached on MT and THF from 8 to 5. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala, can be reached on **(571) 272-7681**. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571)-273-8300.
5. Please note that all future correspondences directed to David L. Lewis must be sent to Art Unit 2629.
6. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner: David L. Lewis
May 30, 2006



BIPIN SHALWALA
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